In re Appln. of Robert C. Phillips, et al.
Application No. 09/638,774

REMARKS

The Office Action dated November 12, 2003, and the references cited therein have been considered. Claims 1-24 are presently pending. No claims currently stand allowed. Applicants have amended the claims to remedy a clarity issue. In view of the remarks set forth herein below, the pending claims 1-24 are patentable over the prior art presently known to Applicants. Accordingly, Applicants request favorable reconsideration of the previous rejection of the now pending claims. Please charge any fee deficiencies to Deposit Account No. 12-1216.

Summary of the Prior Art-Based Claim Rejections

The following identifies the authority and prior art applied to the identified claims for each rejection of the claims set forth in the Office Action dated September 25, 2003.

1. **Sections 7-20**: Claims 1, 2, 7, 9, 11, 12, 13, 14, 19, 21, 23, and 24 are rejected under Section 102(a) as being anticipated by Rierdon et al. U.S. Patent No. 5,978,577 (Rierdon).

2. **Sections 21-24**: Claims 3 and 15 are rejected under Section 103(a) as being unpatentable over Rierdon in view of Basham et al. U.S. Patent No. 6,425,059 (Basham).

3. **Sections 25-27**: Claims 4 and 16 are rejected under Section 103(a) as being unpatentable over Rierdon in view of Basham and Jacobson et al. U.S. Patent No. 5,546,558 (Jacobson).

4. **Sections 28-30**: Claims 5 and 17 are rejected under Section 103(a) as being unpatentable over Rierdon in view of Rungta U.S. Patent No. 6,484,186 (Rungta).

5. **Sections 31-37**: Claims 6, 8, 10, 18, 20 and 22 are rejected under Section 103(a) as being unpatentable over Rierdon in view of Lim et al. U.S. Patent No. 6,374,296 (Lim).

Applicants traverse the grounds for each and every rejection for at least the reasons set forth herein below.

Applicants traverse the rejection, in **Sections 7-20** of Claims 1, 2, 7, 9, 11, 12, 13, 14, 19, 21, 23, and 24 under Section 102(a) as being anticipated by Rierdon. In particular, the invention recited in claim 1 is directed to a distributed multiprocessor architecture including:

an intelligent switch that receives/recognizes all incoming new requests from a WAN bus interface;

a default network processor that receives all initial requests (intelligently directed by the intelligent switch), determines the type of request (e.g., file transfers of particular types – as specified, by way of example on page 17 of the application), and delegates the request to one of a set of specialized request handlers; and

a bus structure/request reassignment tracking logic that support by-passing the default network processor while a particular specialized processor completes the delegated request without intervention by the default processor.

In contrast to the recited invention, the distributed multiprocessor architecture in Rierdon comprises one or more data directory servers (DDSs) that are interposed between a set of servers that actually carry out a request and a network interface through which clients submit the requests. The Office Action proposes that the DDS 150 (in particular the RPC handler executed within the DDS 150 described in column 17) incorporates both the recited "intelligent switch" and the "default handler processor". However, utilizing this interpretation of Rierdon's disclosure proposed by the Office Action, Rierdon does not disclose that the recited "bus structure" and "request reassignment tracking logic" enable completing subsequent communications between the handler processors (data servers 160) and the network interface (105) *"without intervention by the default handler processor"* (DDS 150). Instead, the system disclosed in Rierdon appears to require all communications to *pass through* the DDS 150 (see, col. 17, lines 16-18). For at least this reason, claim 1 is not anticipated by Rierdon.

Applicants furthermore traverse the rejection of independent method claim 13 for at least the reasons set forth above with regard to claims. In particular, Rierdon does not disclose an intelligent switch, bus, and multiprocessor arrangement that would support the recited steps including "bypassing the default handler processor while executing at least a portion of the new request" (carried out by one of the specialized handler processors) – as recited in claim 13.

Applicants traverse the rejection of dependent claims 2, 7, 9, and 12 and 14, 19, 21 and 24 for at least the reason that Rierdon does not disclose a non-blocking switch interposed between a DDS 150 and the Data server(s) 160. Furthermore, with regard to claims 11 and 23, Applicants respectfully request identification of the structure within Rierdon corresponding to

Applicants recited buffer (e.g., SRAM 45) interposed between the data storage facility (e.g., data storage 40) and the specialized processors (26). No such structure appears to be present.

Applicants traverse the rejection in **Sections 21-24** of Claims 3 and 15 under Section 103(a) as being unpatentable over Rierdon in view of Basham. While not contending that version controlled partitions are new, Applicants respectfully submit that using the recited multiprocessor architecture to provide access to such a data storage facility type is neither disclosed nor suggested in the prior art.

Applicants traverse the rejection in **Sections 25-27** of Claims 4 and 16 under Section 103(a) as being unpatentable over Rierdon in view of Basham and Jacobson. In particular, Applicants respectfully submit that the prior art does not disclose using the recited multiprocessor architecture to provide access to a data storage facility that supports incorporating a straddle into storage partitions to facilitate copying stored data assets while maintaining the availability of the stored asset while the data is being copied to a new location.

Applicants traverse the rejection in **Sections 28-30** of Claims 5 and 17 under Section 103(a) as being unpatentable over Rierdon in view of Rungta. Applicants respectfully submit that the prior art does not disclose using the recited bit-map entries to represent the current state of files within the data storage facility that is accessed via the multiprocessor architecture recited in claimed combinations.

Finally, Applicants traverse the rejection in **Sections 31-37** of Claims 6, 8, 10, 18, 20 and 22 under Section 103(a) as being unpatentable over Rierdon in view of Lim. Applicants respectfully submit that while each of the elements, by themselves, may be known, the prior art does not disclose or suggest incorporating the recited elements into a system including the multiprocessor architecture recited within each of these claims.

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Conclusion

The application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

Respectfully submitted,

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